Docket No.: P/63000/Alstom

PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Alan Israel
Reg. No. 27,564

In re: Application of : Jorg-Martin MULLER, et al.

Filed : June 21, 2001

For : DEVICE AND METHOD FOR PROCESSING FREQUENCY SIGNALS

New York, New York
June 21, 2001

PRELIMINARY AMENDMENT

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to calculation of the filing fee and before examination, kindly amend the above captioned application as follows:

IN THE CLAIMS:

Please cancel claims 1-32, without prejudice.

Please add new claims 33-68 as set forth on the enclosed pages.

REMARKS

A new set of claims is provided for the Examiner's approval.

Wherefore, an early action on the merits is earnestly solicited.

Respectfully submitted,

KIRSCHSTEIN, OTTINGER, ISRAEL & SCHIFFMILLER, P.C.
Attorneys for Applicant(s)
489 Fifth Avenue
New York, New York 10017-6105
Tel: (212) 697-3750
Fax: (212) 949-1690

Alan Israel
Registration No. 27,564

PROPOSED NEW SET OF CLAIMS

33. A device for processing an input frequency signal, comprising:

a power limiter including

a) means in a first signal path of the power limiter for analog signal processing of the input signal to generate a first processed signal at an output of the first signal path;

b) means in a second signal path of the power limiter for digital signal processing of the input signal to generate a second processed signal at an output of the second signal path, including means for selective suppression of specific frequency regions in the input signal; and

c) means at the outputs of the first and second signal paths, for combining the first and second processed signals.

34. The device of claim 33, wherein the digital signal processing means includes a finite impulse response (FIR) filter, an analog-to-digital converter at an input to the filter, and a digital-to-analog converter at an output of the filter.

35. The device of claim 34, wherein the filer is operative for adjusting power and delay of the input signal, and for executing a si(x) compensation.

36. The device of claim 34, wherein the filter has a response characteristic having steep sides.

37. The device of claim 34, wherein the converters and the filter operate at a common scanning rate.

38. The device of claim 34, wherein the filter comprises a filter bank.

39. The device of claim 34, wherein the analog signal processing means includes an analog delay element.

40. The device of claim 39, wherein the analog delay element has a constant group delay characteristic.

41. The device of claim 40, wherein the converters and the filter have a total delay characteristic which corresponds to the constant group delay characteristic of the analog delay element.

42. The device of claim 33, wherein the combining means is an analog adder.

43. The device of claim 33; and further comprising an analog-to-digital converter module connected to the combining means of the power limiter.

44. The device of claim 33; and further comprising analog preprocessing means connected to an input of the power limiter, for preprocessing the input signal.

45. The device of claim 44, wherein the analog preprocessing means includes means for feeding a calibration signal to the input signal.

46. The device of claim 43; and further comprising a first complex mixer and a second FIR filter in a third signal path, for digitally implementing an equivalent channel in which a scanning rate reduction occurs.

47. The device of claim 46; and further comprising a second complex mixer and a third FIR filter in a fourth signal path connected to the converter module, for digitally implementing a channel in which a scanning rate reduction occurs.

48. The device of claim 47; and further comprising second means for combining outputs of the third and fourth signal paths.

49. The device of claim 48; and further comprising feedback means for feeding a feedback signal from the converter module to one of the filters via a calibration unit.

50. The device of claim 48; and further comprising feedback means for feeding a feedback signal from the converter module to an adjustable amplifier in the converter module via a calibration unit.

51. A method of processing an input frequency signal, comprising the steps of:

a) analog signal processing of the input signal in a first signal path of a power limiter to generate a first processed signal at an output of the first signal path;

b) digital signal processing of the input signal in a second signal path of the power limiter to generate a second processed signal at an output of the second signal path, including the step of selective suppression of specific frequency regions in the input signal; and

c) combining the first and second processed signals at the outputs of the first and second signal paths.

52. The method of claim 51, wherein the digital signal processing step includes providing a finite impulse response (FIR) filter, an analog-to-digital converter at an input to the filter, and a digital-to-analog converter at an output of the filter.

53. The method of claim 52, wherein the filter is operative for adjusting power and delay of the input signal, and for executing a si(x) compensation.

54. The method of claim 52, wherein the filter has a response characteristic having steep sides.

55. The method of claim 52, wherein the converters and the filter operate at a common scanning rate.

56. The method of claim 52, wherein the filter comprises a filter bank.

57. The method of claim 52, wherein the analog signal processing step includes providing an analog delay element.

58. The method of claim 57, wherein the analog delay element has a constant group delay characteristic.

59. The method of claim 58, wherein the converters and the filter have a total delay characteristic which corresponds to the constant group delay characteristic of the analog delay element.

60. The method of claim 51, wherein the combining step is performed by an analog adder.

61. The method of claim 51; and further comprising the step of connecting an analog-to-digital converter module to the power limiter.

62. The method of claim 51; and further comprising the step of preprocessing the input signal.

63. The method of claim 62, wherein the analog preprocessing step includes feeding a calibration signal to the input signal.

64. The method of claim 61; and further comprising the step of providing a first complex mixer and a second FIR filter in a third signal path, for digitally implementing an equivalent channel in which a scanning rate reduction occurs.

65. The method of claim 64; and further comprising the step of providing a second complex mixer and a third FIR filter in a fourth signal path connected to the converter module, for digitally implementing a channel in which a scanning rate reduction occurs.

66. The method of claim 65; and further comprising the step of combining outputs of the third and fourth signal paths.

67. The method of claim 66; and further comprising the step of feeding a feedback signal from the converter module to one of the filters via a calibration unit.

68. The method of claim 66; and further comprising the step of feeding a feedback signal from the converter module to an adjustable amplifier in the converter module via a calibration unit.